What is claimed is:

1. A method for manufacturing metal lines of semiconductor device, the method comprising the steps of:

forming a first interlayer insulating film exposing a top portion of a lower metal line on a semiconductor substrate;

forming a stacked structure of a first etch barrier film, a second interlayer insulating film, a second etch barrier film, a third interlayer insulating film and an anti-reflection film;

etching the stacked structure to form a via contact hole exposing a portion of the first interlayer insulating film on the lower metal line;

removing the exposed portion of the first interlayer insulating film to expose the lower metal line;

forming a photoresist film on the entire surface;

subjecting the photoresist film to an exposure and development process using an upper metal line mask to form a photoresist film pattern for defining an upper metal line region, wherein the photoresist film pattern further fills a portion of the via contact hole;

etching the anti-reflection film and the third interlayer insulating film using the photoresist film pattern as a mask to form the upper metal line region;

removing the photoresist film pattern; and

forming an upper metal line contacting the lower metal line by filling the upper metal line region.

2. The method according to claim 1, wherein the first and the second etch barrier films comprise a film selected from the group consisting of SiN film, SiC film and SiCN film, respectively.

3. The method according to claim 1, wherein the second and the third interlayer insulating films comprises a film selected from the group consisting of a silica-base low-k film and a silica-base porous low-k film, respectively.

4. The method according to claim 1, wherein the second and the third interlayer insulating films comprises a film selected from the group consisting of an oxide film, an organic low-k film, an organic porous low-k film and combinations thereof, respectively.

5. The method according to claim 1, wherein the anti-reflection film comprises a SiON inorganic anti-reflection film.

6. The method according to claim 1, wherein the step

of etching the anti-reflection film and the third interlayer insulating film is a plasma etching process using a mixture gas of $CF_4/O_2/Ar$.

7. The method according to claim 6, wherein the step of removing the photoresist film pattern in the via contact hole is performed in in-situ manner.